APPLICATION FOR UNITED STATES PATENT

FOR

PROGRAMMABLE SONET
FRAMING

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PROGRAMMABLE SONET FRAMING

Field of the Invention

5   The present invention pertains to the field of networking. More particularly, this

invention relates to programmably framing Synchronous Optical Network (SONET)

frames.

Background

Fiber optics have provided a substantial increase in the volume of data that

10   networks can carry. Synchronous Optical Network (SONET) is a standard that defines

data transmissions over fiber optics. SONET defines a number of different data rates

for different levels of service. A typical SONET network can carry from about 52

megabits per second up to about 10 gigabits per second over a single optical fiber. In

comparison, a typical analog modem operating at maximum efficiency can achieve a

15   mere 56 Kilobits per second. At the 10 gigabit SONET rate, a single optical fiber can

carry enough data to handle well over 100,000 simultaneous voice calls. SONET

networks are likely to carry even larger volumes of data in the future.

Data in a SONET network is often processed in electrical form. For instance, a

SONET network may be made up of a web of optical fibers interspersed with routers

20   and/or switches. The routers and/or switches determine which path data should take to

reach a particular destination. Optical data is usually converted to electrical form before

being processed by a router or switch. If a router or switch determines that data is to

continue on through the SONET network, the data is converted back to optical form

before being passed on to the next router or switch. Data may pass through many

25   routers and/or switches between a source and a destination.

Data is also converted to and/or from optical form at the edges of a SONET network. For example, routers and/or switches may connect one or more electrical networks to one or more SONET networks. Data may start out in electrical form to travel over wires making up an electrical network, get converted by routers and/or

5　switches back and forth between electrical and optical form while traveling among various SONET networks and/or additional electrical networks, and eventually travel in electrical form over wires leading to a destination.

Each time data enters or leaves a SONET network, or gets processed in electrical form within a SONET network, the data is usually converted to/from a

10　particular SONET frame format. The frame format depends on the physical characteristics of the particular SONET medium. Different media can support different sizes of SONET frames, and therefore different volumes of data.

In the past, the electrical hardware used to convert data to and/or from SONET frames has been matched to the corresponding physical SONET medium. That is, if

15　the SONET medium supports 52 megabits per second, a framer is used that converts frames at 52 megabits per second. If the SONET medium supports 10 gigabits per second, a framer is used that converts frames at 10 gigabits per second. If, for any reason, a different data rate is needed or desired, new hardware is required, often requiring considerable additional expense.

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BRIEF DESCRIPTION OF THE DRAWINGS

Examples of the present invention are illustrated in the accompanying drawings. The accompanying drawings, however, do not limit the scope of the present invention. Similar references in the drawings indicate similar elements.

5   Figure 1 illustrates one embodiment of a single-plane SONET frame.

Figure 2 illustrates one embodiment of a composite SONET frame having 192 planes.

Figure 3 illustrates one embodiment of a router.

Figure 4 illustrates one embodiment of a SONET networking card.

10   Figure 5 illustrates one embodiment of a SONET PMD card.

Figure 6 illustrates one embodiment of a SONET output processor.

Figure 7 illustrates one embodiment of simulation environment.

Figure 8 illustrates one embodiment of hardware testing.

DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, those skilled in the art will understand that the present invention may be practiced without

5   these specific details, that the present invention is not limited to the depicted embodiments, and that the present invention may be practiced in a variety of alternate embodiments. In other instances, well known methods, procedures, components, and circuits have not been described in detail.

Parts of the description will be presented using terminology commonly employed

10   by those skilled in the art to convey the substance of their work to others skilled in the art. Also, parts of the description will be presented in terms of operations performed through the execution of programming instructions. As well understood by those skilled in the art, these operations often take the form of electrical, magnetic, or optical signals capable of being stored, transferred, combined, and otherwise manipulated through, for

15   instance, electrical components.

Various operations will be described as multiple discrete steps performed in turn in a manner that is helpful in understanding the present invention. However, the order of description should not be construed as to imply that these operations are necessarily performed in the order they are presented, or even order dependent. Lastly, repeated

20   usage of the phrase "in one embodiment" does not necessarily refer to the same embodiment, although it may.

The present invention provides the flexibility to program the size of a Synchronous Optical Network (SONET) frame. In one embodiment, hardware used to

convert a data stream to and/or from SONET frames uses counters to count the number of byte positions in a SONET frame. The present invention provides programming access to one or more of the counters so that the number of bytes per frame can be changed.

5   By programming the size of SONET frames, a variety of standard SONET data rates may be supported by a single SONET framer. For instance, if a data port on a router is originally coupled to a SONET medium that supports one data rate, and the SONET medium is later changed to a different data rate, it may be possible to reprogram the SONET framer to support the new data rate, saving the cost of replacing

10   the SONET framer with new hardware. A user may even be able to reprogram the framer himself or herself, avoiding the cost and inconvenience of a service call. Furthermore, a supplier may be able to support multiple data rates with one piece of hardware, eliminating the cost and inconvenience of stocking different hardware for each data rate.

15   Programmable frame sizes can also be used to improve a variety of testing and hardware development situations. For instance, high speed SONET hardware tends to be fairly complex. Designs are usually created and tested in a simulation environment prior to costly fabrication. At the 10 gigabit data rate, a single SONET frame includes about 155 thousand bytes. A software simulator may take hours to simulate the

20   framing of a single frame of data. Once the design of the framer has been tested and verified, continuing to simulate the framing of huge frames of data may be unnecessary for the verification of other components of the design. By programming the framer for a

smaller frame size, the simulation time needed to design and test the other components can be substantially reduced.

Programmable frame size can similarly improve the performance of a hardware emulator. A hardware emulator is made up of hardware elements that can be

5   programmed to represent the functionality of circuit designs. For instance, a circuit design can be written in a hardware description language, such as Verilog, and loaded into an emulator to model the design. Hardware emulators tend to be much faster than software simulators. But, as fast as hardware emulators are, the programmable hardware elements tend to be less efficient than actual SONET hardware. At a high

10 SONET data rate, such as the 10 gigabit rate, even an emulator may be bogged down by the volume of data, and may benefit from smaller frame sizes.

Programmable frame size can be helpful when testing the actual hardware of a SONET framer as well. For instance, a logic analyzer can be used to capture and analyze data from the actual hardware. At the 10 gigabit rate, the volume of data in a

15 single frame is so large that a logic analyzer may only be able to capture part of a single frame, making it very difficult to test the functionality of the hardware across frame boundaries. By programming the framer for smaller frame sizes, the logic analyzer may be able to capture and analyze several frames of data, exposing the functionality at frame boundaries and allowing the framer to cycle through more operational states in a

20 shorter period of time.

Programmable frame size can also be helpful when developing hardware and/or software surrounding a SONET framer. For instance, if a new hardware component for processing SONET overhead is needed, and the overhead processor needs to operate

on the same data stream as the SONET framer, it may be desirable to simulate or emulate the overhead processor and couple the modeled design to the actual SONET framer. Any number of simulator or emulator interfaces can be used. The simulator or emulator may not be fast enough to handle the maximum data rate supported by the

5   framer. In which case, the framer could be programmed to a lower data rate to match the speed of the simulator or emulator.

Figure 1 illustrates one embodiment of a single-plane SONET frame. The SONET frame is 9 rows high by 90 columns wide. Each entry in the frame is an 8 bit byte. Transmitting the data in a frame begins at row 1, column 1 and ends at row 9,

10   column 90. Bits of data are transmitted serially, one at a time, as pulses of light in an optical fiber. The frame is read across rows from left to right, one row at a time.

Frames are written in the illustrated format so that overhead bytes and payload bytes are easily identified. Bytes in the first three columns, columns 110, are reserved for overhead bytes, and bytes in the remaining columns, columns 120, are payload

15   bytes. When the data is transmitted serially, the first three bytes are overhead, the next 87 bytes are payload, the next three bytes are overhead, the next 87 bytes are payload, and so on.

Some additional byte positions in one column among the payload bytes may also be used for overhead. In the illustrated embodiment, the additional overhead bytes 130

20   are in column 4 of the payload section. In alternate embodiments, the additional overhead bytes can be in any column in the payload section, and may not occupy an entire column. All of the overhead bytes, including those in columns 110, are used to

manage various operations in a SONET network, such as routing, error checking, and the like.

Figure 2 illustrates one embodiment of a composite SONET frame. The composite frame is comprised of multiple planes identical to the single-plane frame illustrated in Figure 1. That is, each plane in the composite frame includes 9 rows and 90 columns, with up to 36 bytes of overhead. In the illustrated embodiment, there are 192 planes in the frame.

The composite frame is read from front to back, and then left to right. That is, the byte in row 1, column 1 is read from each plane, starting with plane 1 and ending with plane 192. Then, the bytes in row 1, column 2 are read from all 192 planes, followed by the bytes in row 1, column 3 from all 192 planes, and so on. As the composite frame is read serially, the data stream comprises 9 iterations (one iteration for each row) of 576 bytes of overhead (from 192 planes times 3 overhead bytes per row) followed by 16704 bytes of payload (from 192 planes times 87 payload bytes per row). Somewhere among each 16704 bytes of payload there are also up to 192 continuous bytes of payload that are used for overhead, depending on the logical construction of the composite frame.

The composite frame of Figure 2, like the single-plane frame of Figure 1, is a single unit in the SONET network. That is, no matter how many planes a frame has, one frame is transmitted every 125 micro seconds, or 8000 times per second. By increasing the size of a frame by adding more planes, the data rate increases. For instance, the data rate for the single-plane frame of Figure 1 is 810 bytes per frame times 8 bits per byte times 8000 frames per second, which equals 51.84 Megabits per

second. For the 192-plane frame of Figure 2, the data rate is 810 bytes per plane times 192 planes per frame times 8 bits per byte times 8000 frames per second, which equals 9.95328 Gigabits per second.

The frame format for the 192 plane frame of Figure 2 is referred to as optical carrier level 192 (OC-192). The optical carrier level corresponds to the number of planes in the frame. OC-192 is a standard SONET frame size that provides the 10 gigabit data rate. Other standard SONET frame sizes that provide lower data rates include OC-3 (156 megabits/second), OC-12 (625 megabits/second), and OC-48 (2.5 gigabits/second).

A SONET framer converts a data stream to a stream of SONET frames by filling available payload bytes locations with data bytes from the data stream and filling byte locations reserved for overhead with overhead bytes generated by other components. A SONET framer recovers a data stream in the opposite way.

In one embodiment, a SONET framer includes three counters, a row counter, a column counter, and a plane counter. The values of the counters define the current byte position in a frame, and depending on the byte position, the framer knows whether a byte is payload or overhead.

Figure 3 illustrates one embodiment of a router 300 that can take advantage of the present invention. Router 300 includes a number of networking cards 320. In the illustrated embodiment, each network card includes three physical medium dependency (PMD) cards 330. Each PMD card 330 has input/output ports to couple the router 300 to a physical network medium. PMD cards 330 may couple the router to any number of electrical wire networking media, wireless networking media, and, of course, optical

fiber media for SONET networking. The optical fiber media may include fibers that support a variety of optical carrier levels, such as OC-3, OC-12, OC-48, and OC-192.

Router 300 also includes data fabric 310. As data is received from a physical networking media, the corresponding PMD card 330 and networking card 320 convert

5   the data to a format that is usable by data fabric 310. Data fabric 310 then directs the data to one of the various output ports. A networking card 320 and PMD card 330 corresponding to the selected output port convert the data to a format supported by the physical networking medium.

When physical network media are added, deleted, or replaced, the networking

10   cards 320 and PMD cards 330 are changed to accommodate the physical media. For changes in SONET optical carrier level, the present invention makes it possible to change the card by simply reprogramming the networking card 320 to support the new physical media rather than replacing the entire card.

Except for the teachings of the present invention, router 300 is tended to

15   represent a wide variety of networking devices known in the art. Alternate embodiments may include any number of input/output ports dispersed among any configuration of networking cards and PMD cards. In alternate embodiments, the present invention may similarly be used with any number of SONET devices, such as signal regenerators, switches, and the like.

20   Figure 4 illustrates one embodiment of a SONET networking card 410 in more detail. The networking card 420 includes a router interface 420, and three pairs of SONET processors 440 and corresponding PMD slots 430 to couple the router to three SONET networks. In the past, if any one of the SONET networks changed, it would be

necessary to replace the entire card, potentially at great expense. However, with the present invention, a single card can be programmed to support several different SONET physical media. Rather than replacing the entire card when one physical medium changes, the corresponding SONET processor 440 can be reprogrammed to

5   support the new medium.

Alternate embodiments of SONET networking cards may include any number of PMD card slots. Generally, the more slots a networking card provides, the more expensive the card is to replace, making reprogrammability that much more desirable.

Figure 5 illustrates one embodiment of a SONET PMD card 510 in more detail.

10   PMD card 510 is intended to represent a wide variety of such devices known in the art. Such devices tend to be relatively simple and inexpensive. In the illustrated embodiment, the card includes an electro/optical converter 530 and a clock generator 540. Electro/optical converter 530 converts framed data 550 to and from optical data 520. Converter 530 is "matched" to the physical medium of the network. That is,

15   SONET data is transmitted synchronously, at a constant data rate. Converter 530 sends and receives data at both the electrical and optical sides according to the data rate dictated by the optical carrier level of the physical medium.

Clock generator 540 generates clock signals 560 for internal use and for the corresponding SONET processor. In one embodiment, clock signals 560 include a

20   frame synchronization signal and a data clock. SONET frames are sent at a constant synchronous rate, 8 kHz, no matter what the optical carrier rate is. In which case, a universal frame synchronization signal is provided throughout a SONET network. Clock generator 540 passes the frame synchronization signal to the SONET processor and

derives the data clock from the frame synchronization signal. The data clock is dictated by the data rate of the optical carrier level of the physical network medium. Since SONET frames are built one byte at a time, the data clock is usually derived such that it cycles once for each byte of data. In which case, the data clock for OC-192 would be

5   approximately 1.2 gigahertz.

Figure 6 illustrates one embodiment of a SONET processor, processor 600, for processing an output data stream. The same processing happens in reverse for an input data stream. In the illustrated embodiment, processor 600 includes overhead processor 610 and framer 620. Overhead processor 610 performs a wide variety of

10   SONET processing known in the art. Framer 620 combines data stream 628 from the router with various overhead bytes from overhead processor 610 to provide framed data 660 to the PMD card at the constant data rate dictated by the optical carrier level of the SONET medium.

In order to provide framed data 660 at the dictated rate, framer 620 receives a

15   frame sync signal 624 and a data clock 626. Frame sync 624 may be received from the PMD card, from some other source, or, in an alternate embodiment, may be generated internally. Similarly, data clock 626 may be received from the PMD card, from some other source, or, in an alternate embodiment, may be generated internally.

Framer 620 starts a new frame for each frame sync signal 624. That is, row

20   counter 630, column counter 640, and plane counter 650 all start from one. Plane counter 650 is incremented for each clock cycle of data clock 626. Column counter 640 is incremented each time plane counter 650 reaches its maximum value and returns to one. Row counter 630 is incremented each time column counter 640 reaches its

maximum value and returns to one. Depending on the byte position in the SONET

frame indicated by the values of the three counters, framer 620 loads either a byte from

data stream 628 or a byte of overhead into framed data 660 for each clock cycle of data

clock 626.

5   Except for the teachings of the present invention, framer 620 represents any of a

number of such devices known in the art. In alternate embodiments, any number of

techniques can be used to identify byte locations in frames. For instance, one alternate

approach uses two counters rather than three, and represents byte locations in SONET

frames in two dimensions.

10   According to the teachings of the present invention, one or more of the counters

within framer 620 are programmable. Inventive framer 620 also includes program

interface 622 to program the programmable counter(s). Program interface 620 may be,

for instance, a data bus coupled to a processor. In which case, software can be used

to program the counter(s) by writing to particular address spaces corresponding to the

15   counter(s). Alternately, program interface 620 may represent any number of interfaces,

including one or more dip switches or the like.

Where plane counter 650 is programmable, framer 620 can be programmed to

support multiple standard SONET data rates. For instance, in one embodiment, the

default setting for plane counter 650 is 192, to support OC-192. However, by

20   reprogramming plane counter 650 to 48, 12, or 3, the SONET processor 600 can

support OC-48, OC-12, or OC-3, respectively. Row counter 630 and column counter

640 do not need to be programmable to support any of these standard data rates

because the plane dimensions are 9 rows by 90 columns for each standard data rate.

If the framer is only programmable to support four different standard SONET

data rates, program interface 622 could comprise a pair of dip switches to represent the

four possible modes of operation. Alternately, software could write a two bit register

value to the framer to select one of the four possible modes of operation. Of course,

5   any number of approaches can be used for program interface 622, including directly

writing the desired maximum number of planes to the programmable plane counter.

Under certain circumstances, it can be useful to program framer 620 to generate

non-standard frames. In which case, plane counter 650 may be programmed to a non-

standard number of planes. Furthermore, row counter 630 and/or column counter 640

10   may also be programmable to provide non-standard plane dimensions. For instance,

each time the number of rows is reduced by one, the frame size is reduced, and

therefore the volume of data per frame is reduced, by almost 17 thousand bytes.

Reducing the volume of data may be helpful when testing or designing various

components. However, reducing the number of rows may cut off some needed

15   overhead bytes. In which case, it may be more desirable to keep the number of rows,

but reduce the number of columns. By reducing the maximum number of columns, the

payload portion of a frame can be trimmed without loosing overhead bytes. In other

situations, it may be beneficial to change any combination of rows, columns, and

planes.

20   Figures 7 and 8 illustrate some situations in which it can be useful to reprogram

the frame size to various sizes, including non-standard frame sizes. In Figure 7,

simulation environment 710 is used to model a circuit design 720. Simulation

environment may include software simulation, hardware emulation, and the like. If

circuit design 720 models the framing of a large SONET frame, it may take an

excessively long time to simulate. For instance, in software simulation, an OC-192

frame may several hours to simulate. Once framing has been tested and verified, it

may be possible to speed up the testing and verification of other components in design

5   720 by programming the frame size to reduce the volume of data being modeled.

Furthermore, if design 720 represents components that interact with a SONET

framer, it may be beneficial to model the components in conjunction with the actual

SONET framer hardware component 730 through simulation environment interface 740.

Any number of co-simulation environments can be used to couple simulation

10   environment 710 to hardware component 730. Again, it may be possible to speed up

the testing and verification of design 720 by programming the frame size to reduce the

volume of data being modeled.

In Figure 8, hardware component 810 includes a SONET framer. The hardware

component is analyzed by logic analyzer 820. That is, logic analyzer 820 provides

15   various test vectors to hardware component 810 to cycle the hardware through various

operational states. Logic analyzer captures and analyzes the hardware responses to

the test vectors. At the OC-192 data rate, the logic analyzer may only be able to

capture and analyze a portion of a single frame. By reducing the frame size, logic

analyzer 820 may be able to capture data from multiple frames, thereby cycling through

20   more operational states more efficiently and in less time.

In one embodiment, the present invention, as described above, is implemented

as part of an application specific integrated circuit (ASIC) for SONET protocol

processing. The software described above for programming frame sizes could be

implemented in code running on an embedded controller, an external processor, or the like, as will be comprehended by a person skilled in the art. In another example, field programmable gate arrays (FPGAs) or static programmable gate arrays (SPGA) could be used to implement one or more functions of the present invention. In yet another

5   example, a combination of hardware and software could be used to implement one or more functions of the present invention.

Thus, programmable SONET framing is described. Whereas many alterations and modifications of the present invention will be comprehended by a person skilled in the art after having read the foregoing description, it is to be understood that the

10   particular embodiments shown and described by way of illustration are in no way intended to be considered limiting. Therefore, references to details of particular embodiments are not intended to limit the scope of the claims.